

**What is claimed is:**

**[Claim 1]** 1. A connection device capable of converting a pixel clock to a character clock, the connection device comprising:

a pixel clock generator for generating a pixel clock having a number of cycles that is not an integer multiple of a first number during a predetermined interval;

a frequency divider for generating a character clock according to the pixel clock; and

a logic unit for controlling the frequency divider to generate the character clock by dividing the number of cycles of the pixel clock during part of the predetermined interval by the first number and by dividing the number of cycles of the pixel clock during the remaining part of the predetermined interval by a second number.

**[Claim 2]** 2. The connection device of claim 1 wherein the logic unit makes the number of cycles of the character clock generated by the frequency divider an integer.

**[Claim 3]** 3. The connection device of claim 1 wherein the first number is eight or nine.

**[Claim 4]** 4. The connection device of claim 1 wherein the second number is the number of cycles of the pixel clock during the remaining part of the predetermined interval.

**[Claim 5]** 5. A method for converting a pixel clock to a character clock, the method comprising:

providing a pixel clock with a number of cycles that is not an integer multiple of a first number during a predetermined interval; and

dividing the number of cycles of the pixel clock during part of the predetermined interval by the first number and dividing the number of cycles of the pixel clock during the remaining part of the predetermined interval by a second number for generating the character clock.

**[Claim 6]** 6. The method of claim 5 wherein the number of cycles of the character clock generated by dividing the pixel clock during the predetermined interval is an integer.

**[Claim 7]** 7. The method of claim 5 wherein the first number is eight or nine.

**[Claim 8]** 8. The method of claim 5 wherein the second number is the number of cycles of the pixel clock during the remaining part of the predetermined interval.